AMENDMENT

In the Claims:

Please amend claims 11 and 15 as follows.

11. (Amended) A NAND logic circuit having a first input and a second input, comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator layer;

a p-well formed in said semiconductor layer;

a first gate structure formed atop said p-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said p-well, said second gate structure being the ~~first~~ second input and being formed from a thin gate oxide layer underneath a conductive layer;

a p+ structure formed adjacent to a first edge of said first gate structure and said second gate structure, said p+ structure being the output of said NAND logic circuit;

an n+ structure formed adjacent to a second edge of said first gate structure and said second gate structure;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said p+ structure.

5 15. (Amended) A NAND logic circuit having a first input and a second input, comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator layer;

B2 a n-well formed in said semiconductor layer;

a first gate structure formed atop said n-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said n-well, said second gate structure being the ~~first~~ second input and being formed from a thin gate oxide layer underneath a conductive layer;

a n+ structure formed adjacent to a first edge of said first gate structure and said second gate structure;

a p+ structure formed adjacent to a second edge of first gate structure and said second gate structure, said p+ structure being the output of said NAND logic circuit;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input.

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